REMARKS

The application has been carefully reviewed in light of the Office Action dated November 30, 2004. Applicant gratefully acknowledges the Examiner's statement that claims 3-9 and 12 contain allowable subject matter. Claims 1 and 10 have been amended. Claims 1-12 remain presently pending in this application.

Claims 1, 2, 10 and 11 stand rejected under 35 U.S.C. § 102(e) as being anticipated U.S. Patent No. 6,608,771 to Jacobson et al. Applicant respectfully traverses this rejection and requests reconsideration.

Amended claim 1 recites, *inter alia*, a method for detecting a mismatch in a content addressable memory (CAM) comprising "charging a matchline of a match detection circuit of said CAM to a first voltage level different than a ground potential." Claim 1 also recites "changing the voltage level of said matchline to a second voltage level if the logic state of [a] first bit does not match the logic state of [a] second bit, said second voltage level being different than said first voltage level and different than said ground potential."

Jacobson does not disclose these limitations. In fact, Jacobson explicitly states that "[t]he first potential is ground and the second potential is VDD. Alternatively, the first potential is VDD and the second potential is ground," Col. 3, lines 22-24. Amended claim 1 recites that both the first and second voltage levels are different than ground potential. At least for these reasons, claim 1 is allowable over Jacobson and the rejection should be withdrawn.

Claim 2 depends from claim 1 and is allowable for at least the same reasons stated above, and also because Jacobson fails to teach or suggest the inventive combination defined by claim 2.

Amended claim 10 recites, *inter alia*, a method for detecting a mismatch in a content addressable memory (CAM) comprising "charging a matchline of a match detection circuit of said CAM to a first voltage level different than a ground potential." Claim 10 also recites "changing the voltage level of said matchline to a second voltage level if the logic state of at least one of [a] second plurality of bits does not match the logic state of its corresponding bit in [a] first plurality of bits, said second voltage level being different than said first voltage level and higher than said ground potential."

The deficiencies of Jacobson have been discussed above. Claim 10 is allowable over Jacobson at least for the same reasons mentioned above.

Claim 11 depends from claim 10, and is allowable for at least the same reasons stated above, and also because Jacobson fails to teach or suggest the inventive combination defined by claim 11.

Applicant also notes claims 3-9 and 12, indicated as containing allowable subject mater, define further unique combinations of limitations not found in the prior art. Therefore, the stated reasons for the indication of allowable subject matter should be interpreted as highlighting only some of the reasons why the claims are allowable. As usual, the scope of the claims should be interpreted based on the actual language of the allowed claims, and no further limitation of the claims should be inferred from the Examiner's statements.

In view of the above, Applicant respectfully submits that the application is in condition for allowance.

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Respectfully submitted,

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